What is claimed is:

1. A ground plane for a semiconductor chip adapted to be mounted on a supporting member in a chip package, wherein said ground plane comprises at least one first capacitor plate provided within said chip, and at least one second capacitor plate provided on said supporting member, said first and second capacitor plate being separated by a dielectric layer and capacitively coupled to each other via this layer, and said ground plane comprising at least one first conducting member, said first conducting member being at least one electrically conducting via extending through said supporting member and electrically coupled in series with said second capacitor plate.

2. Ground plane according to claim 1, wherein the resonant frequency of the capacitance provided by said first capacitor plate and said second capacitor plate, and the inductance provided by said first conducting member, is approximately equal to the intended working frequency of said chip.

3. Ground plane according to claim 1 or 2, wherein the dielectric layer is an integral part of said chip.

4. Ground plane according to claim 3, wherein said dielectric layer covers the entire surface of the chip facing the supporting member.

5. Ground plane according to claim 3 or 4, wherein said dielectric layer comprises silicon oxide.

6. Ground plane according to one of the proceeding claims, wherein said second capacitor plate comprises a layer of conductive glue.

7. Ground plane according to any of the preceding claims, wherein said capacitor plate is a metallic layer on said supporting member.

8. Ground plane according to claims 6 and 7, wherein said layer of conductive glue is provided between said metallic layer and said dielectric layer.

9. Ground plane according to one of the proceeding claims, wherein said at least one electrically conducting via extending through said supporting member is directly connected to the second capacitor plate.

10. Ground plane according to claim 7, 8 or 9, wherein said vias and said metallic layer are integrally formed from the same metal.

11. Method for providing a ground plane for a semiconductor chip mounted on a supporting member in a chip package, characterised in providing a metal covered area on the surface of said supporting member, providing a number of vias electrically connected to said metal covered area and extending therefrom through said supporting to the opposite side thereof, connecting in parallel at least two of said number of vias.

12. Method for providing a tuned ground plane for a semiconductor chip mounted on a supporting member in a chip package according to claim 10, wherein the semiconductor chip is adhered to said supporting member by means of a conductive glue.

13. Semiconductor chip package comprising a semiconductor chip and a supporting member, said supporting member comprising at least one metal covered area and at least one electrically conductive via extending from said metal covered area through said supporting member, wherein said chip is adhered to the supporting member by means of conductive glue and that said conductive glue is in electrical contact with said metal covered area.

14. LC series circuit for a semiconductor chip substantially as herein before described with reference to figs. 1-4 of the accompanying drawings.

15. Method for providing a tuned RF-ground plane for a semiconductor chip mounted on a supporting member in a chip package substantially as herein before described with reference to figs. 9-10 of the accompanying drawings.

16. Semiconductor chip package comprising a semiconductor chip and a supporting member substantially as herein before described with reference to figs. 1-4 of the accompanying drawings.

Add A3

Add B1